IDEC Chip Design Contest

A 12b 50MS/s 0.18μm CMOS SAR ADC Based on Highly Linear C-R Hybrid DAC

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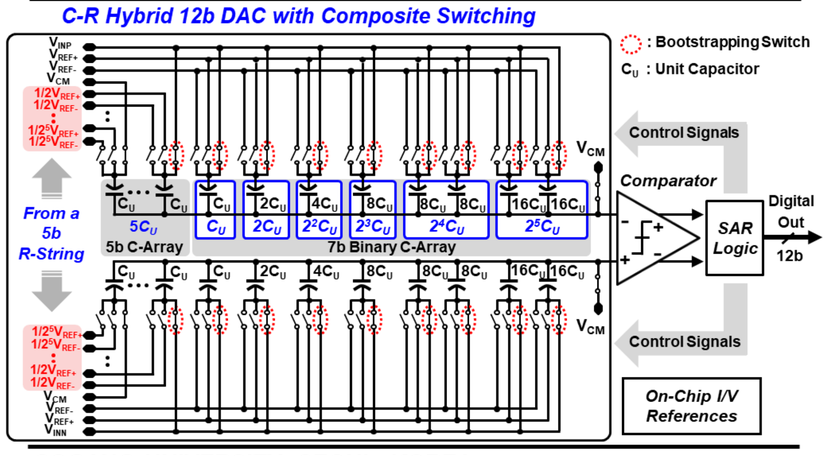
INTRODUCTION

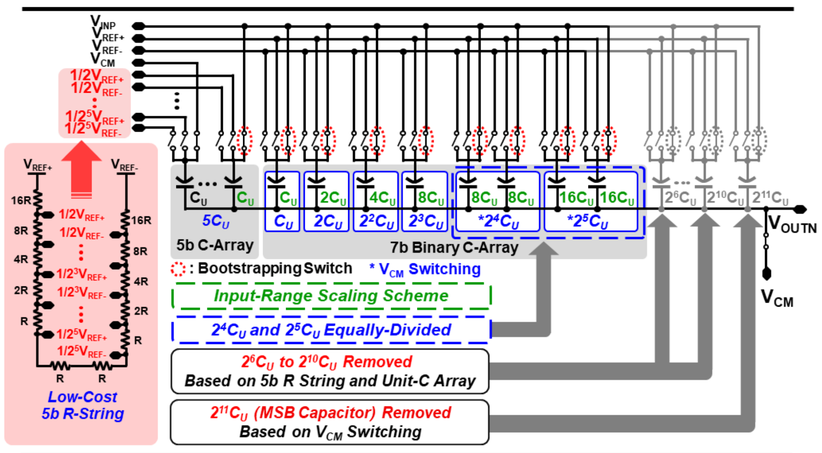
- Required ADC specifications for intelligent semiconductor system applications:
  - Resolution : 12b ➤ Sampling rate : 50MS/s
  - Small chip area and low power consumption in CMOS process
- Conventional monotonic switching of SAR ADCs :
  - Simple circuit topology and SAR operation with top plate sampling
  - Dynamic offset caused by V_{CM} variations of a DAC output
  - Non-competitive switching power of a DAC
- *Proposed 12b 50MS/s SAR ADC based on a 0.18μm CMOS process :*
  - Composite switching composed of V_{CM} and monotonic switching in sequence
  - Composite switching simultaneously to minimize switching power of a DAC and dynamic offset caused by V_{CM} variations of a DAC output
  - Back-end 5b R-string for 5 LSBs combined with a unit C-array in the DAC for small chip area
  - Input-range scaling to match an input range exactly to the reference voltage range without extra or dummy capacitors

PROPOSED 12b 50MS/s SAR ADC

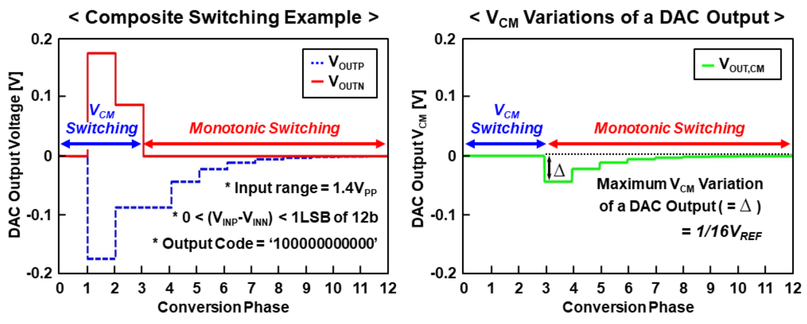
C-R Hybrid 12b DAC with Composite Switching



DETAILED C-R HYBRID DAC TOPOLOGY

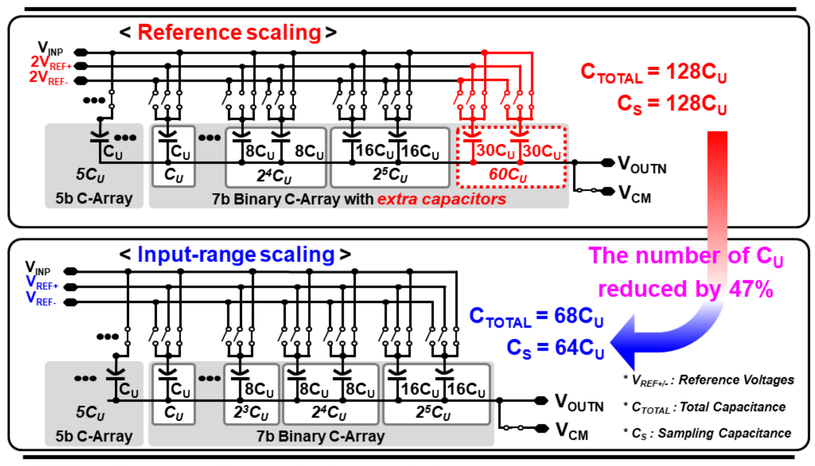


PROPOSED COMPOSITE SWITCHING

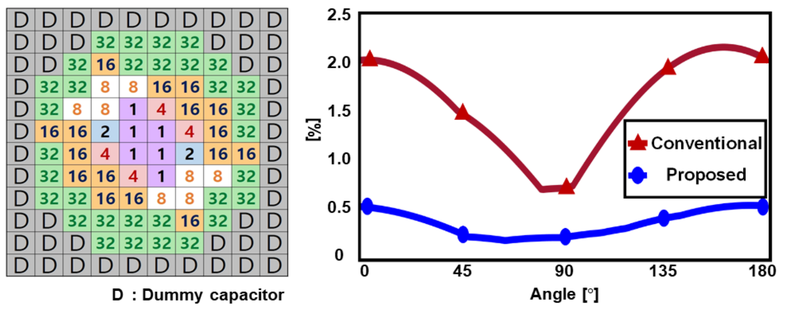


- Composite switching composed of V_{CM} and monotonic switching in a consecutive order
- V_{CM} variations of a DAC output guaranteed within $1/16V_{REF}$ with composite switching

PROPOSED INPUT-RANGE SCALING SCHEME

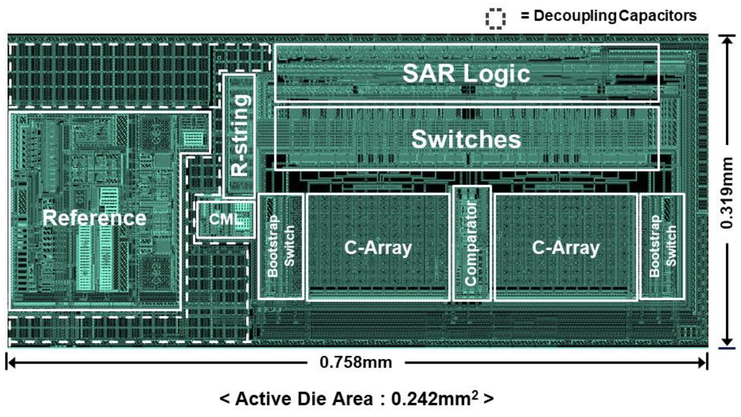


MISMATCH-MINIMIZED CAPACITOR PLACEMENT



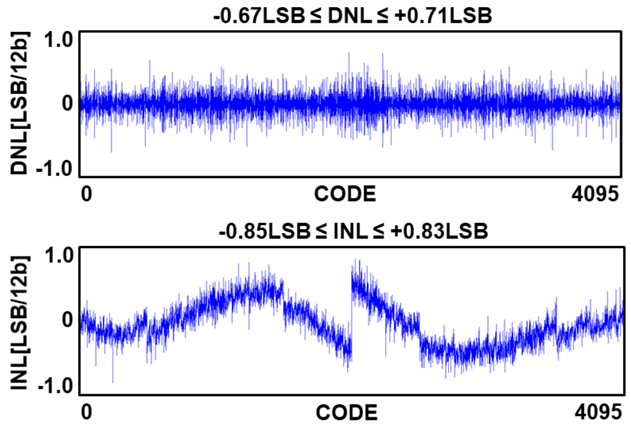
- More careful placement of C_U needed to minimize capacitor mismatch
- Common-centroid placement typically used to reduce oxide-gradient-induced mismatch

LAYOUT OF THE PROTOTYPE ADC

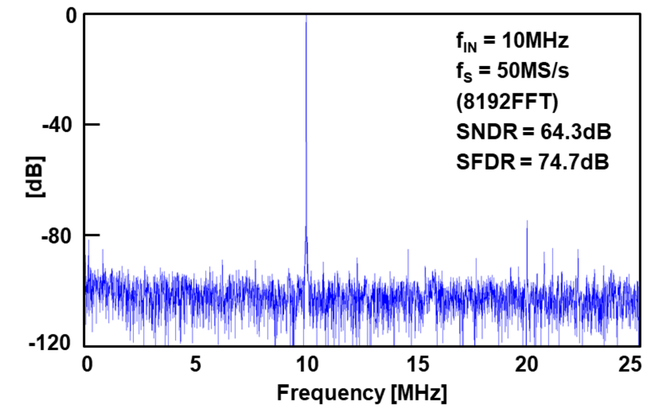


< Active Die Area : $0.242mm^2$ >

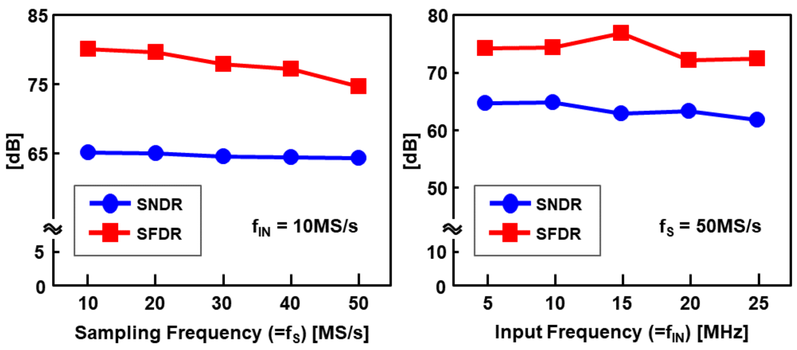
MEASURED STATIC PERFORMANCE



MEASURED DYNAMIC PERFORMANCE



MEASURED SNDR & SFDR vs. f_S & f_{IN}



MEASURED ADC PERFORMANCE

Resolution	12bits
Conversion Rate	50MS/s
Process	MagnaChip 0.18μm CMOS
Supply	1.8V
Input Range	$1.4V_{P-P}$ (differential)
DNL	-0.67LSB / +0.71LSB
INL	-0.85LSB / +0.83LSB
SNDR	64.3dB (@ f_{IN} = 10MHz) / 61.1dB (@ f_{IN} = 25MHz)
SFDR	74.7dB (@ f_{IN} = 10MHz) / 72.6dB (@ f_{IN} = 25MHz)
ADC Power	4.74mW (w/o I/V REF) / 6.73mW (with I/V REF)
Active Die Area	$0.165mm^2$ (w/o I/V REF) / $0.242mm^2$ (with I/V REF)

COMPARISON TO THE PREVIOUS ADCs

	Resol. [bits]	Speed [MS/s]	Supply [V]	Power [mW] (@ Current)	Area [mm^2]	Number of Unit Cap.	Cal.	SNDR [dB]	FoM [fJ/conv.]	Process [CMOS]
This Work	*12*	*50*	*1.8*	*4.74 (2.63mA)*	*0.17*	*136*	*X*	*64.3*	*70.6*	*0.18μm*
TCASI'16	12	10	1.8	0.82 (0.46mA)	0.36	4096	X	66.9	44.2	0.18μm
APCCAS'18	12	20	1.5	1.22 (0.81mA)	0.10	300	X	61.7	59.6	0.18μm
TCASI'18	12	20	1.8	1.77 (0.98mA)	1.61	2048	O	64.6	63.7	0.18μm
TVLSI'18	12	40	1.2	1.32 (1.10mA)	0.10	280	X	62.5	30.4	0.13μm
JSSC'15	12	35	1.1	0.42 (0.38mA)	0.06	1024	O	60.9	13.2	40nm

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